FIG 1

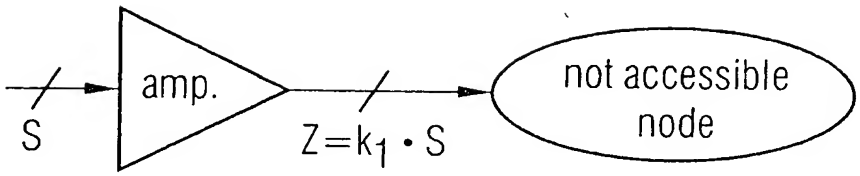


FIG 2
Prior Art

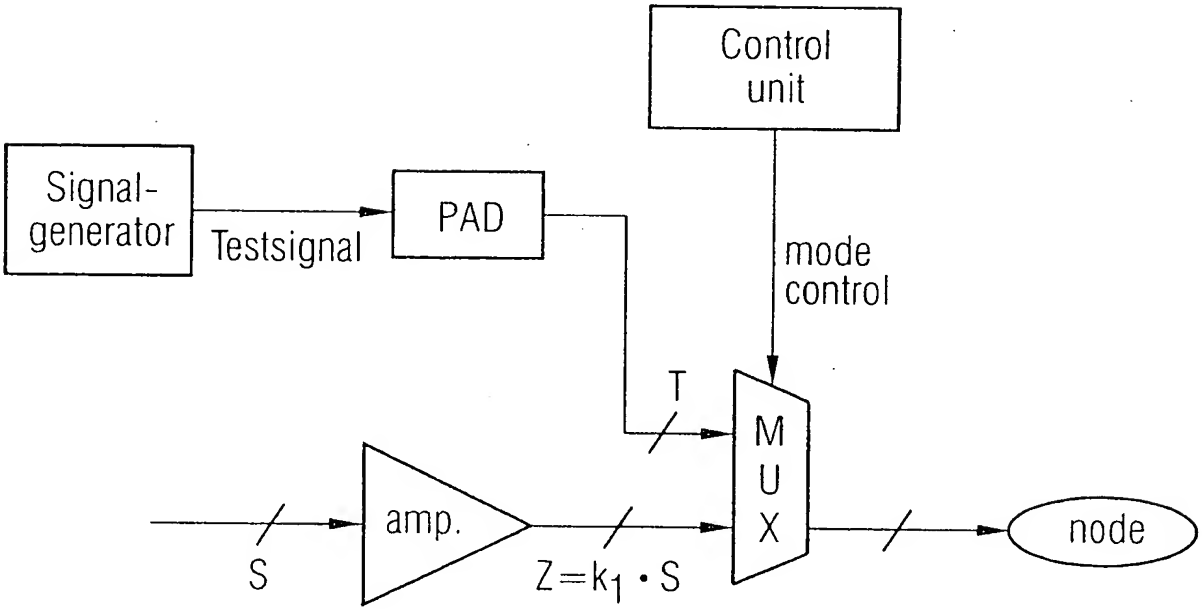


FIG 3
Prior Art

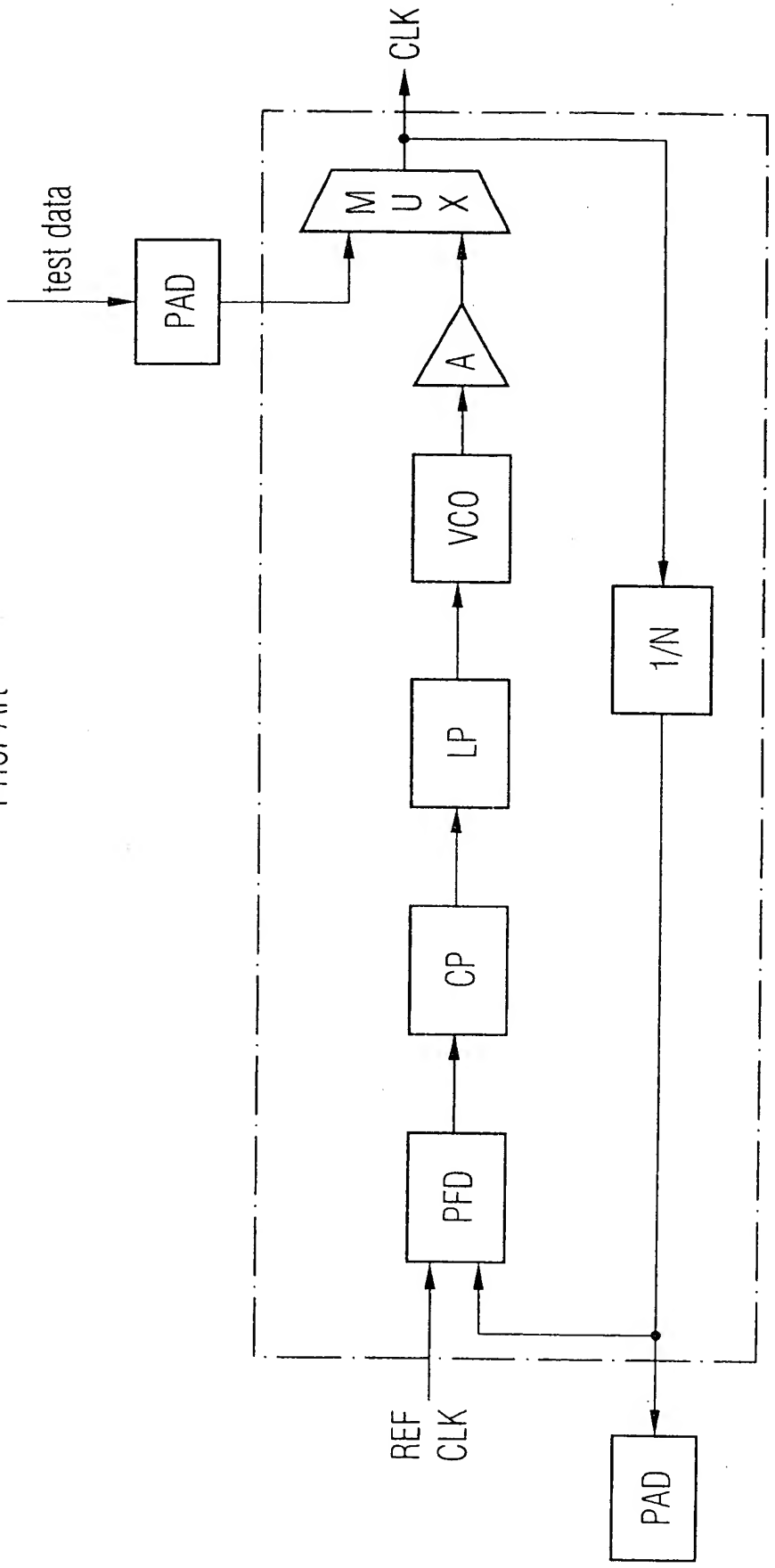


FIG 4

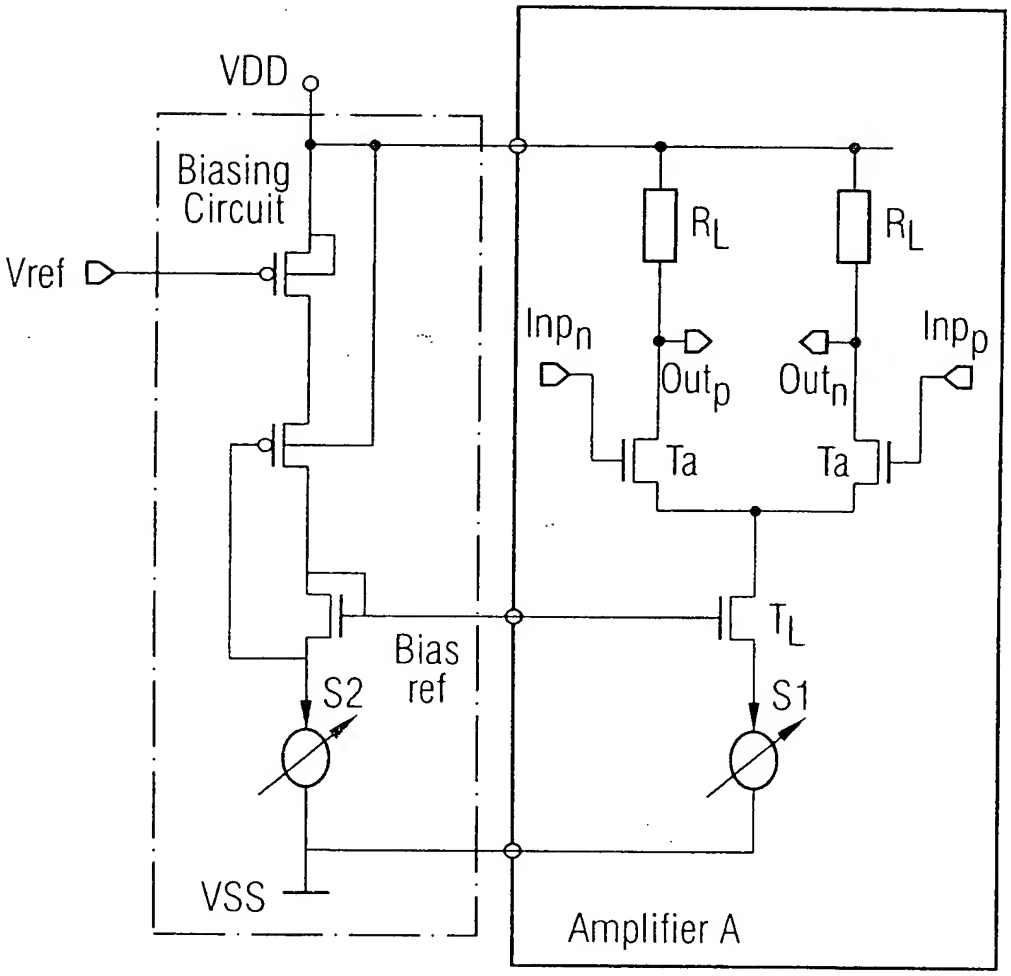
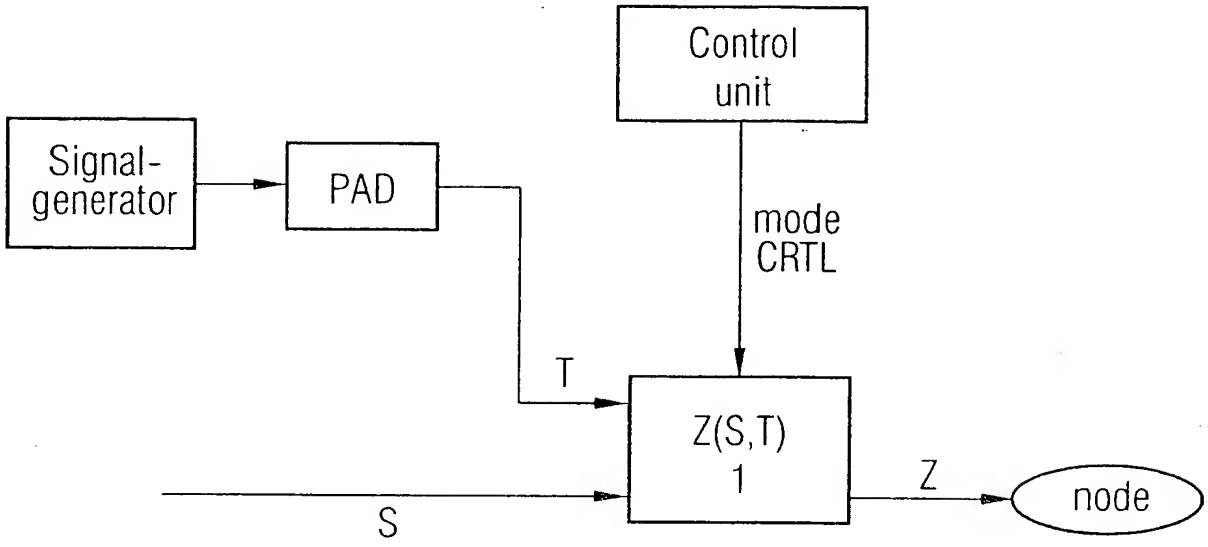

VDD
Biasing Circuit
Vref
Bias ref
S2
S1
VSS
R_L
R_L
Inp_n
Out_p
Out_n
Inp_p
Ta
Ta
T_L
Amplifier A

FIG 5



$$Z(S,T) = k_1 S + k_2 T \quad \text{normal mode}$$
$$Z(S,T) = k_3 S + k_4 T \quad \text{test mode}$$

FIG 6

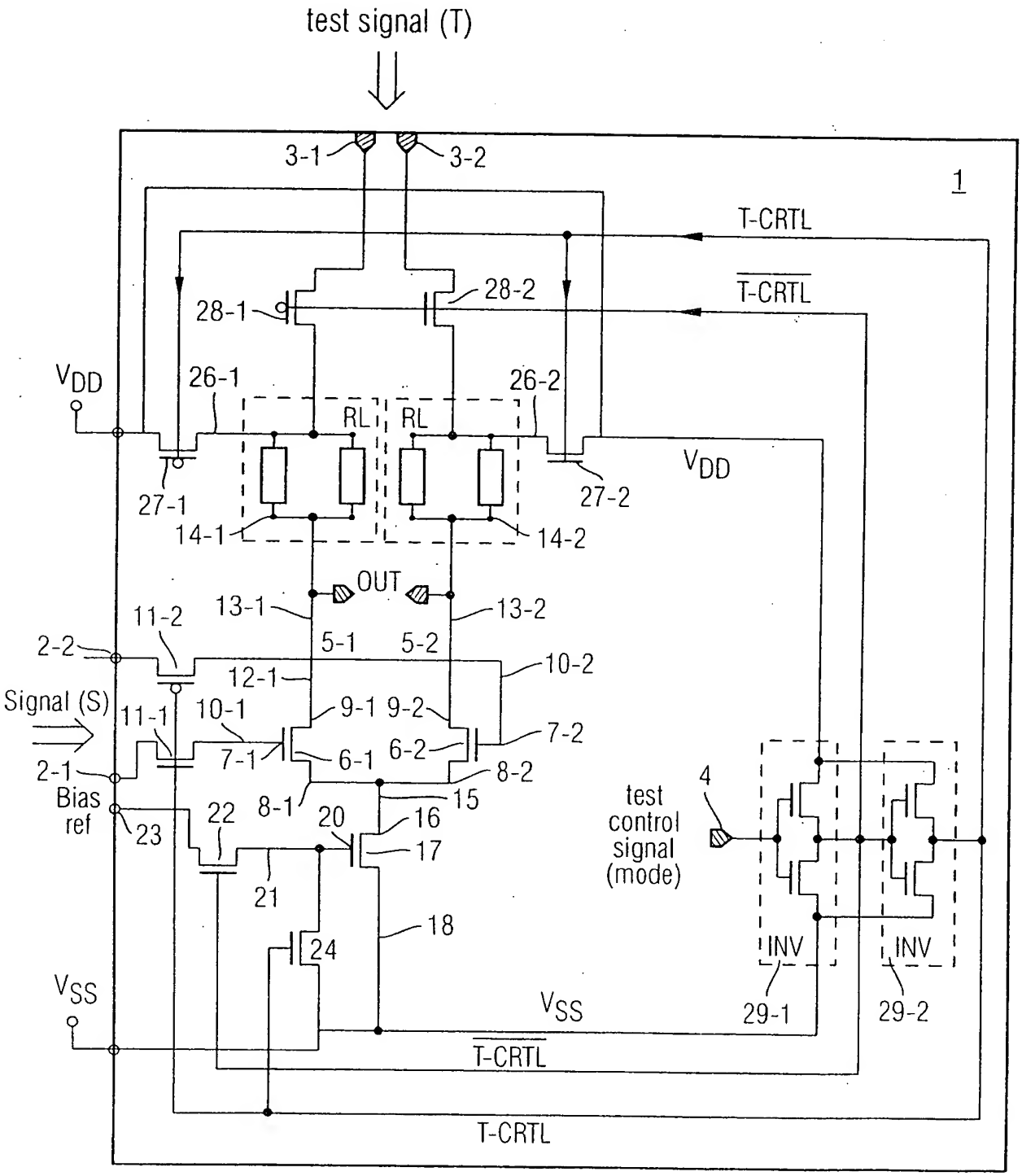

test signal (T)
3-1
3-2
1
T-CRTL
$\overline{\text{T-CRTL}}$
28-1
28-2
V_{DD}
26-1
26-2
RL
RL
27-1
27-2
14-1
14-2
OUT
13-1
13-2
11-2
2-2
5-1
5-2
10-2
12-1
Signal (S)
11-1
10-1
9-1
9-2
7-2
7-1
6-1
6-2
8-2
2-1
Bias ref
23
22
8-1
20
16
15
17
21
18
24
V_{SS}
$\overline{\text{T-CRTL}}$
T-CRTL
4
test control signal (mode)
INV
INV
29-1
29-2

FIG 7A

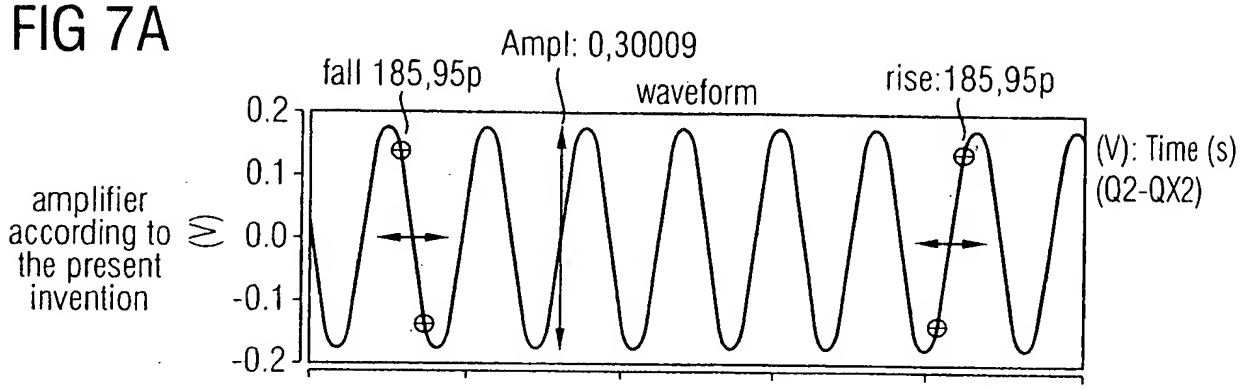


FIG 7B

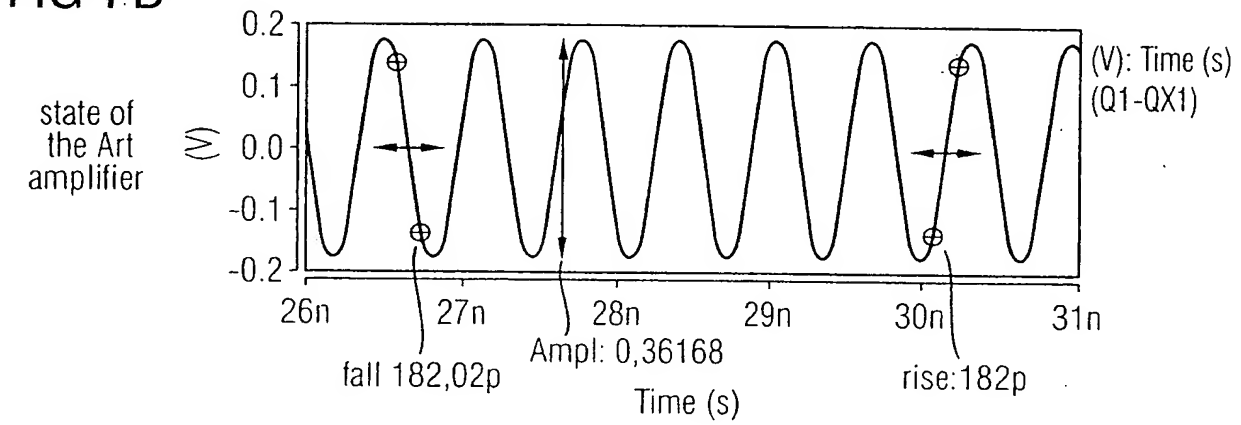


FIG 8

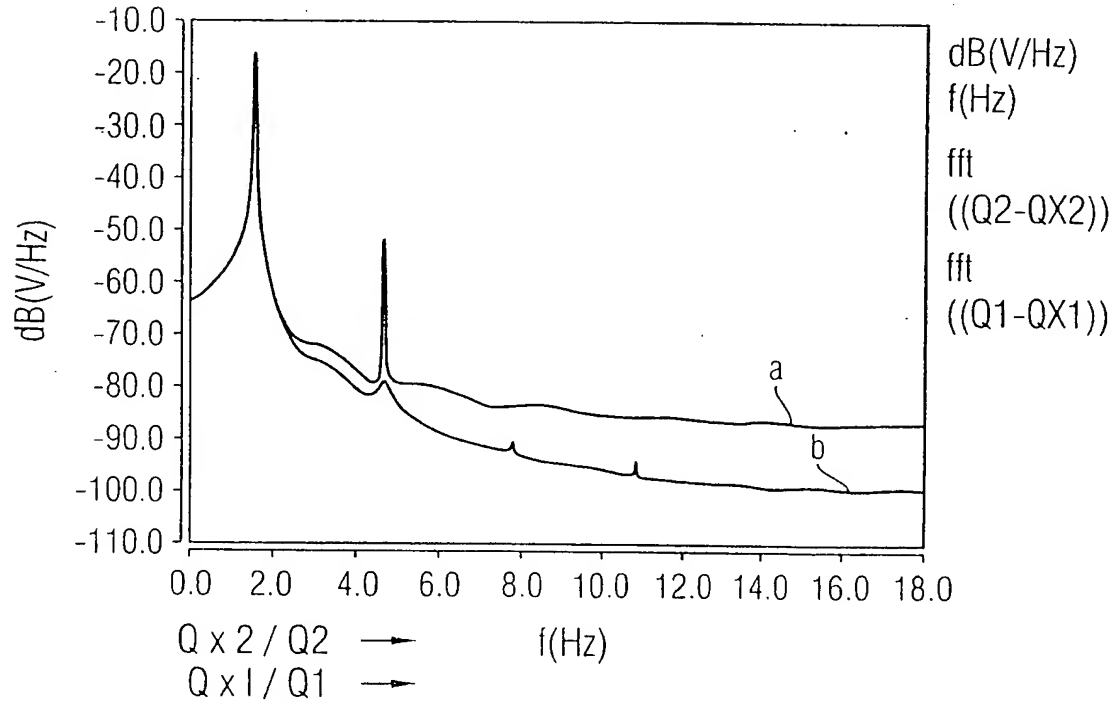


FIG 9

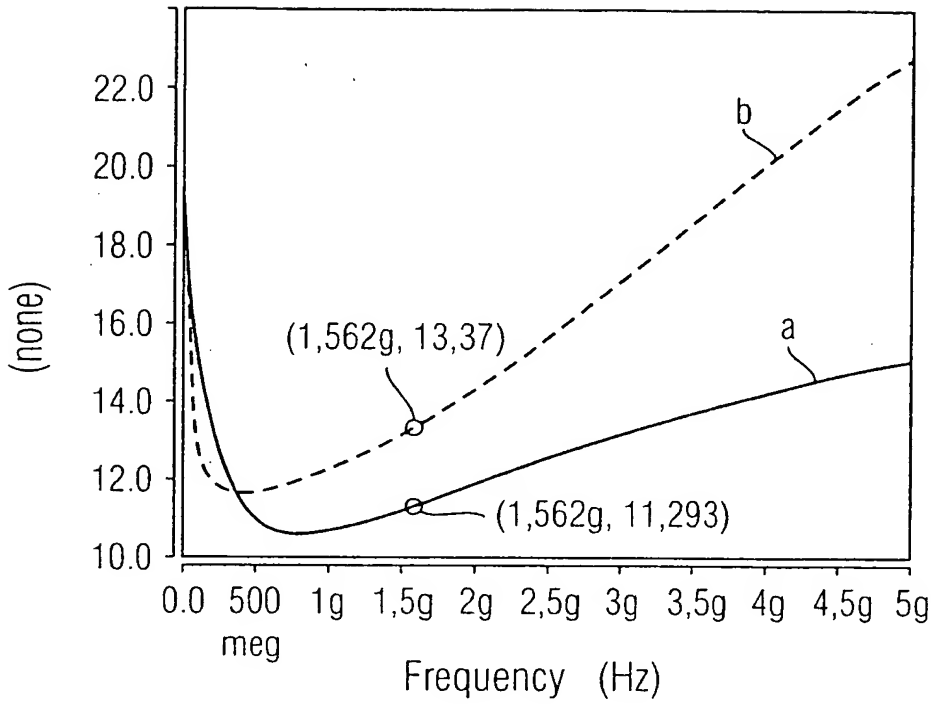

22.0
20.0
18.0
16.0
14.0
12.0
10.0
(none)
b
a
(1,562g, 13,37)
(1,562g, 11,293)
0.0 500 1g 1,5g 2g 2,5g 3g 3,5g 4g 4,5g 5g
meg
Frequency (Hz)

FIG 10

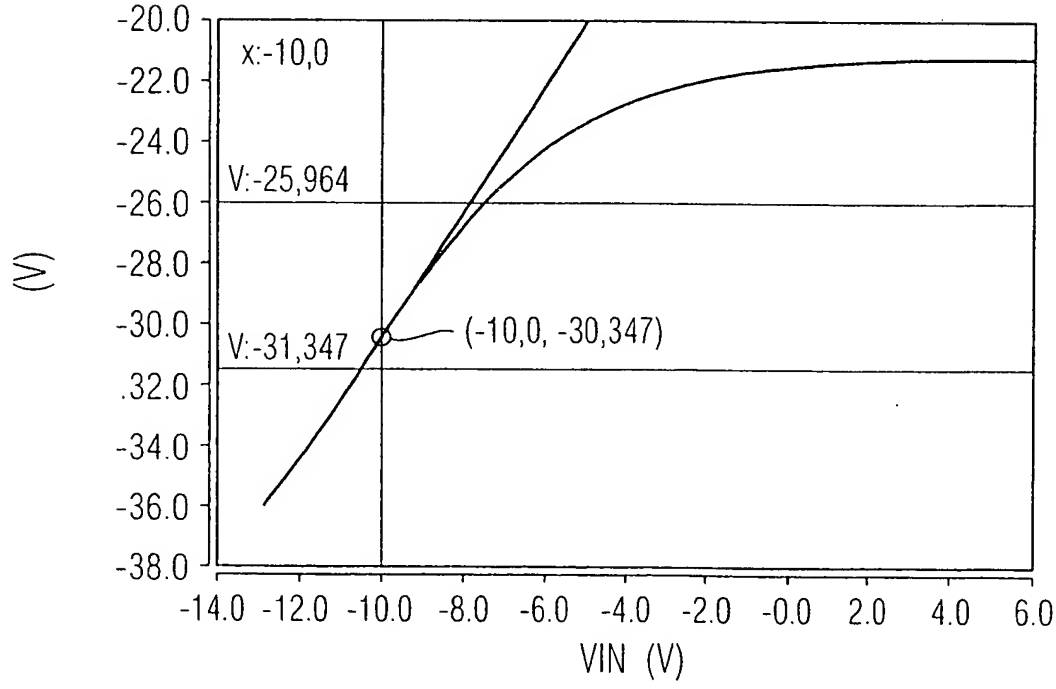

-20.0
-22.0
-24.0
-26.0
-28.0
-30.0
.32.0
-34.0
-36.0
-38.0
(V)
x:-10,0
V:-25,964
V:-31,347
(-10,0, -30,347)
-14.0 -12.0 -10.0 -8.0 -6.0 -4.0 -2.0 -0.0 2.0 4.0 6.0
VIN (V)

FIG 11

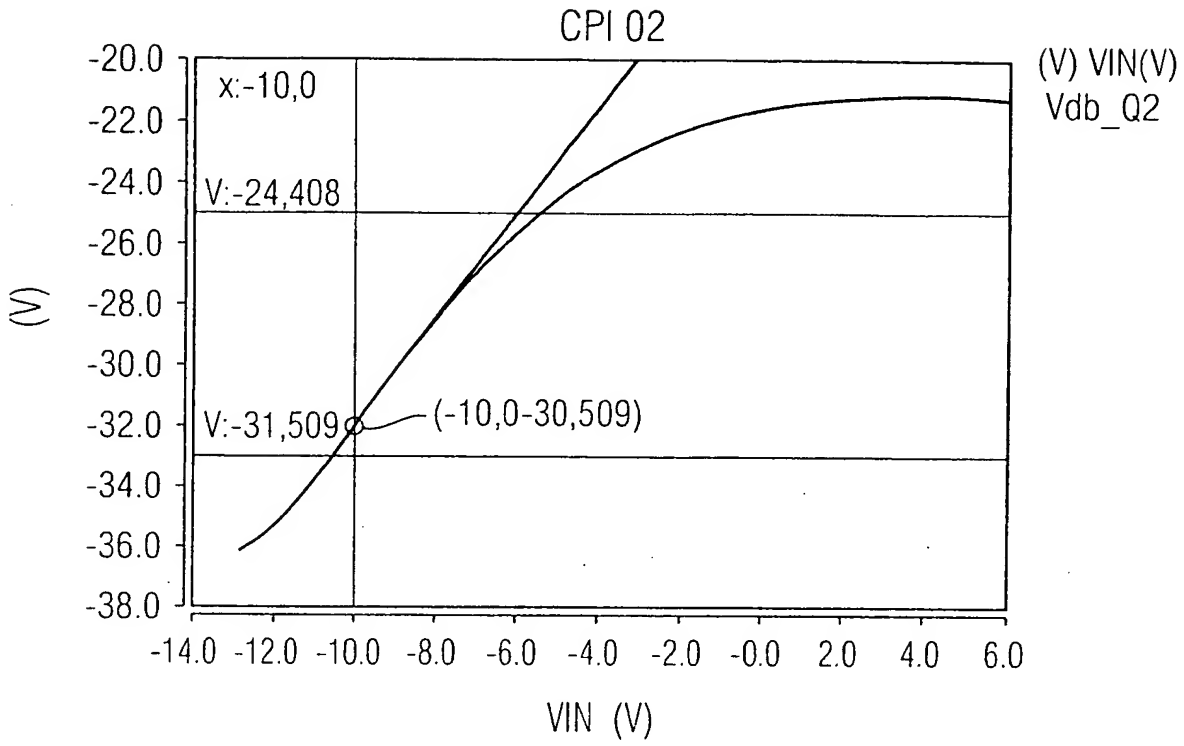

CPI 02
(V) VIN(V)
Vdb_Q2
x:-10,0
V:-24,408
V:-31,509
(-10,0-30,509)
-20.0
-22.0
-24.0
-26.0
-28.0
-30.0
-32.0
-34.0
-36.0
-38.0
(V)
-14.0 -12.0 -10.0 -8.0 -6.0 -4.0 -2.0 -0.0 2.0 4.0 6.0
VIN (V)

FIG 12

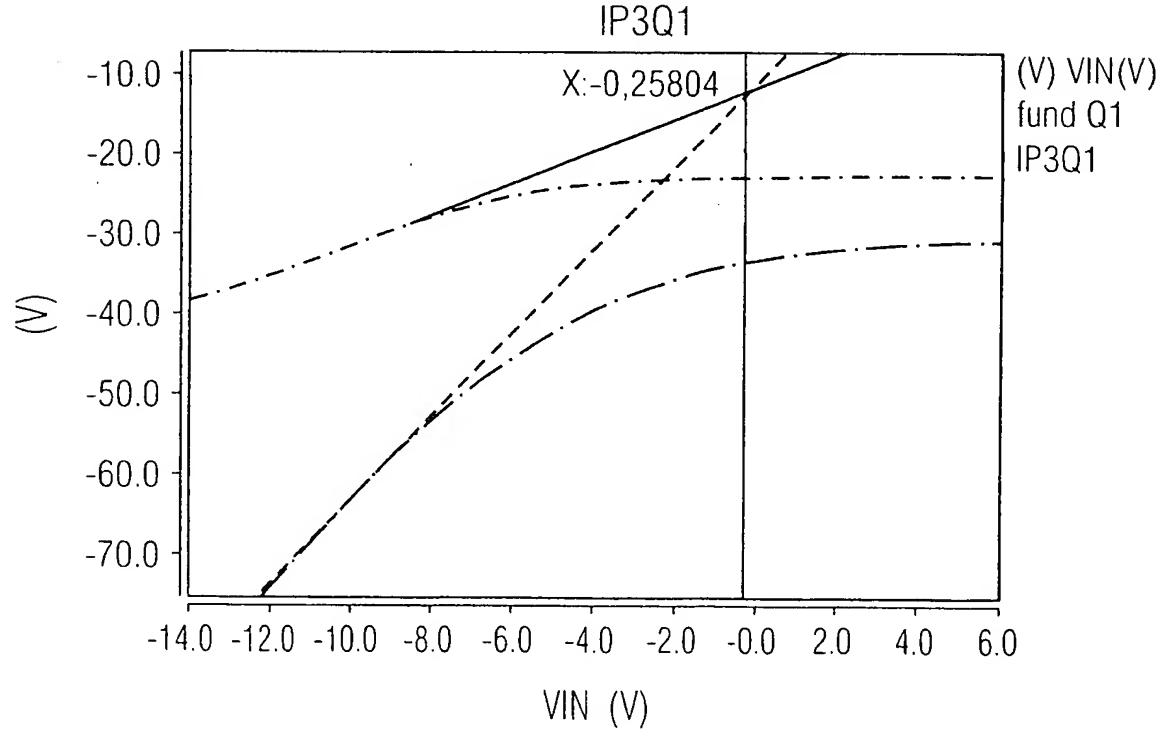
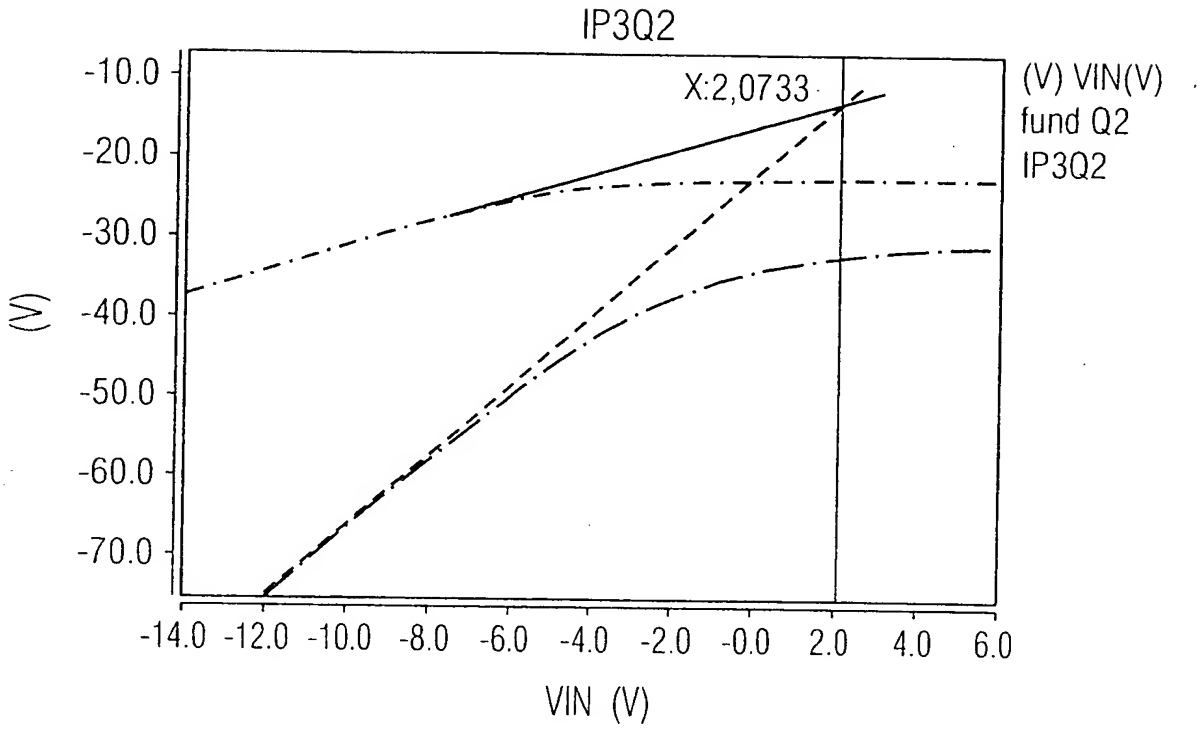

IP3Q1
X:-0,25804
(V) VIN(V)
fund Q1
IP3Q1
-10.0
-20.0
-30.0
-40.0
-50.0
-60.0
-70.0
(V)
-14.0 -12.0 -10.0 -8.0 -6.0 -4.0 -2.0 -0.0 2.0 4.0 6.0
VIN (V)

FIG 13


IP3Q2
X:2,0733
(V) VIN(V)
fund Q2
IP3Q2
-10.0
-20.0
-30.0
-40.0
-50.0
-60.0
-70.0
(V)
-14.0 -12.0 -10.0 -8.0 -6.0 -4.0 -2.0 -0.0 2.0 4.0 6.0
VIN (V)